WHAT IS CLAIMED IS:

1. An Integrated Circuit (IC), comprising:

a plurality of modules:

a scan chain combiner coupled to the output of each one of said plurality of modules for selecting one value per scan chain received from said plurality of modules, said value indicative of errors in any of said plurality of modules: and

an output test mux for communicating said value to a tester via a plurality of chip outputs.

2. The Integrated Circuit of claim 1, further including a plurality of chip inputs for receiving test signals from said tester.

3. The Integrated Circuit of claim 2, wherein said test signals comprise test vectors.

4. The Integrated Circuit of claim 1, wherein said scan chain combiner utilizes majority voting logic for comparing the outputs of each one of said plurality of modules to each other.

5. The Integrated Circuit of claim 1, wherein each one of said plurality of modules includes a plurality of registers.

6. The Integrated Circuit of claim 1, further comprising scan chain inputs for performing scan testing on the Integrated Circuit.

7. The Integrated Circuit of claim 6, wherein the scan chain inputs are coupled to each one of the plurality of modules via a source pin.

8. The Integrated Circuit of claim 7, wherein the scan chain inputs are coupled to a plurality of pins.

9. The Integrated Circuit of claim 1, further comprising input muxes for communicating a specific module input signal to a respective one of the plurality of modules.

10. The Integrated Circuit of claim 1, wherein said Integrated Circuit comprises an Application Specific Integrated Circuit (ASIC).

11. The Integrated Circuit of claim 2, wherein said test vectors are processed in parallel by the plurality of modules.

12. The Integrated Circuit of claim 10, further comprising a rest of logic portion for performing the design specific operation of the ASIC.

13. The Integrated Circuit of claim 12, further comprising an output mux for dynamically selecting an output from one of the plurality of modules to communicate to the rest of the logic.

14. The Integrated Circuit of claim 13, wherein said output mux includes a scan module select signal for selecting specific scan outputs from one of the N modules.

15. The Integrated Circuit of claim 12, wherein said output mux includes a scan mode signal for informing each one of a plurality of registers that it will be tested.

16. A method of implementing test capabilities for an Integrated Circuit (IC) comprising:

placing the IC into test mode via the test mode signal of the IC;

allocating scan chains to each one of a plurality of modules;

inserting test vectors through the scan chain;

comparing the outputs of the plurality of modules at a scan chain combiner;

selecting a value as an output for the scan chain combiner, said output value being indicative of at least one error in any of said plurality of modules; and

communicating said output value to a tester via an output test mux.

17. The method of claim 16, further comprising:

communicating the output of one of the plurality of modules to other parts of the IC via an output mux.

18. The method of claim 17, wherein the output of the plurality of modules stimulates the rest of the logic portion of the IC.

19. The method of claim 16, wherein the IC is an Application Specific Integrated Circuit (ASIC).

20. The method of claim 16, wherein said step of selecting comprises using majority voting logic.

21. The method of claim 20, wherein said majority voting logic further comprising selecting the value from the plurality of modules that is in the minority.

22. The method of claim 16, further comprising:
comparing the output scan chain value to an expected value.

23. The method of claim 22, wherein a difference between the expected value and the scan chain value comprises an error.

23. The method of claim 22, further comprising:
comparing the output value of each one of the plurality of modules to the expected value in response to finding an error between the expected value and the scan chain value.

24. The method of claim 17, wherein the output of the plurality of modules stimulates one of the other N-1 modules.